REMARKS/ARGUMENTS

Claims 1-13 stand objected to, with claims 1-26 rejected in the outstanding Official Action. In response to the claim objections, Applicants have amended claims 1 and 14 and therefore claims 1-26 remain in this application.

Claims 1-13 stand objected to in section 2, page 2 of the Final Rejection with respect to a newly offered "potential 101 rejection." The Examiner correctly notes that claim 1 is an apparatus claim and suggests that the claim does not recite any hardware for performing the steps of the claim. Applicants note that the previously filed claim recites "an interrupt controller" (corresponds to the "nested vector interrupt controller 24" discussed on page 8, lines 27-34 and elsewhere in the specification and shown in Figure 1). The claimed interrupt controller clearly is a hardware element of the Applicants' claim.

However, in addition, Applicants have offered to amend the language of claim 1 to more positively recite "a processor configured to perform processing operations" rather than the previously recited "processing logic operable to perform processing operations." Applicants' originally filed specification at page 8, lines 15-17 discusses the processor which is claimed and illustrated in the drawings. Applicants have also added the structure of a "stack data store" described on page 11, lines 4-24 and in Figure 3 of the present application.

Thus, Applicants' claim 1, as amended, recites not only the "interrupt controller," but also the "processor" and the "stack data store." All three of the above elements are clearly hardware structures and therefore this amendment clearly obviates any "potential 101 rejection."

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Entry of the Amendments to Claims 1 and 14

Applicants respectfully request entry of the above amendment to claims 1 and 14 inasmuch as they respond to the Examiner's newly voiced "potential 101 rejection" which was not mentioned or present in any previous Official Action. While Applicants have pointed out that claim 1 previously recited the hardware of the "interrupt controller 24" disclosed in Figure 1 of Applicants' specification, Applicants have further amended claim 1 to recite the "processor" and the "stack data store." Thus, Applicants' amended claim 1 clearly recites hardware and claimed interrelationships between hardware, thereby clearly meeting the requirements of 35 USC §101 and obviating any potential §101 rejection.

This amendment could not have been made at an earlier date because the "potential 101 rejection" was not mentioned in any previous Official Action. Entry of this amendment will also obviate any possible §101 rejection in the future or the need for the Board to consider any §101 rejection. Applicant does not add any new claims, nor does Applicant raise new issues requiring further consideration and/or search. As a consequence, the above amendments to claims 1 and 14 should be entered pursuant to the provisions of Rule 116.

Claims 1-7, 10-12, 14-20 and 23-25 stand rejected under 35 USC §103 as unpatentable over Miu (U.S. Patent 4,488,227) in view of Ishimoto (U.S. Patent 5,410,715). Applicants have also amended claims 1 and 14 to address the Examiner's objections in paragraphs 5-8. Specifically, the additional language to claims 1 and 14 focuses the present invention on features of Figure 4 which are described on pages 11 and 12 of the specification. The previously claimed interrupt controller determines a stack priority level corresponding to the highest priority interrupt event among any interrupt events associated with the state data stored in the stack data

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store (see page 12, lines 9-12). In this instance, the interrupt controller detects that the one or more second interrupt events has a higher priority than the processing that was interrupted by the first interrupt event if the one or more second interrupt events have a higher priority than the stack priority level (as discussed on page 12, lines 12-17).

These elements and the claimed interrelationships allows the present invention to address problems that arise when priority levels associated with stack interrupts are programmable (as discussed in the specification between page 11, line 25 and page 12, line 8). When priority levels of stacked interrupts can be altered, then a situation could arise wherein a stacked interrupt is changed to have a higher priority than the interrupt at the top of the stack. This means that execution of the high priority interrupt could be delayed if further interrupts arise which are of higher priority than the interrupt at the top of the stack but lower than the interrupt that was changed to a high priority.

The present invention addresses this problem by determining a stack priority level corresponding to the highest priority interrupt among the interrupts associated with the stacked state data. The interrupt controller then treats the processing that was interrupted by the first interrupt event (corresponding to the data at the top of the stack) as if it had the stack priority level so that the second interrupt event is only determined to have a higher priority than the processing interrupted by the first interrupt event <u>if</u> the second interrupt event has a higher priority than the stack priority level. This means that high priority interrupts are not inappropriately delayed by lower priority interrupts which happen to be located at a higher position in the stack.

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This interrelationship between the priority interrupts and the structures recited in claim 1 and corresponding method steps recited in claim 14, clearly distinguishes over the Miu and Ishimoto references. Miu does not describe any concept of priority levels associated with the interrupts (this is recognized in the Examiner's admission at section 6, page 3 of the Final Rejection, stating that "Miu did not teach detecting one or more higher priority interrupts during the execution of the first interrupt").

Because Miu does not teach detecting higher priority interrupts, it certainly cannot suggest or disclose the newly added features of apparatus claim 1 and method claim 14. While the Ishimoto reference is cited in conjunction with Miu, Ishimoto does not recognize that the priority level of nested interrupts could change after they are stacked.

Ishimoto only compares priority levels of a pending interrupt with an "in-service process priority value" corresponding to the processing currently being performed (see column 4, lines 31-33 and 65-69 in the Ishimoto reference). Ishimoto assumes that processing currently being performed will always have a higher priority than a previously interrupted processing (as recognized by the Examiner in section 32, last two lines, in the Official Action). The present invention of determining a stack priority level corresponding to the highest priority interrupt among the stacked interrupts and treating the data at the top of the stack as if it had the stack priority level would not be obvious from the Miu and Ishimoto references even if they were combined.

Additionally, the Examiner provides no reason for combining portions of the Miu and Ishimoto references in the manner of Applicants' amended claims 1 and 14. In its recent decision, the U.S. Supreme Court in *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385

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(April 2007), held that "[t]o facilitate review [of the Examiner's rationale for combining references], this analysis should be made explicit." *Id.* at 1396.

The Supreme Court in its *KSR* decision went on to say that it followed the Court of Appeals for the Federal Circuit's advice that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (emphasis added, the Supreme Court quoting from the Court of Appeals for the Federal Circuit in *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006)).

Accordingly, there is *prima facie* basis for rejecting claims 1-7, 10-12, 14-20 and 23-25 under 35 USC §103 over the Miu/Ishimoto combination and any further rejection thereunder is respectfully traversed.

Claims 8, 9, 21 and 22 stand rejected under 35 USC §103 over the Miu/Ishimoto combination and further in view of McMahan (U.S. Patent 5,706,491). Inasmuch as claims 8, 9, 21 and 22 depend from independent claims 1 and 14 (at least indirectly), the above comments distinguishing independent claims 1 and 14 from the Miu/Ishimoto combination are herein incorporated by reference.

The Examiner's confirmation that "the combined method of Miu and Ishimoto does not specifically disclose "repairing to undo any partial return call" (section 20, Final Rejection) is appreciated. However, there is no allegation that the additional McMahan reference discloses the missing structures and interrelationships noted above in independent claims 1 and 14 and therefore even if Miu, Ishimoto and McMahan were combined, they would not necessary

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disclose the subject matter of independent claims 1 and 14 or claims 8, 9, 21 and 22 dependent thereon.

Moreover, the Examiner has failed to provide any explicit "analysis" of how or why one of ordinary skill in the art would pick and choose elements from the Miu/Ishimoto/McMahan references and then combine them in the manner of Applicants' independent claims or dependent claims 8, 9, 21 and 22. Accordingly, any further rejection of these claims under 35 USC §103 is respectfully traversed.

Claims 13 and 26 stand rejected under 35 USC §103 as unpatentable over the Miu/Ishimoto combination, further in view of Raasch (U.S. Patent 5,237,692). As claims 13 and 26 ultimately depend from claims 1 and 14, the above comments with respect to claims 1 and 14 are herein incorporated by reference.

The Examiner does not allege that the newly added Raasch reference discloses the missing elements from the Miu and Ishimoto combination noted with respect to claims 1 and 14 and therefore even if the Miu/Ishimoto/Raasch references were combined, they do not make out a *prima facie* case of obviousness for the subject matter of claims 1 and 14 or even narrower claims 13 and 26 dependent thereon.

Additionally, the Examiner has not met his burden of providing a *prima facie* basis for combining references as there is no explicit "analysis" of the rationale for picking and choosing elements from the Miu/Ishimoto/Raasch references and then combining those elements in the manner of Applicants' dependent claims 13 and 26. Accordingly, any further rejection of claims 13 and 26 is respectfully traversed.

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It is noted that the above amendments to independent claims 1 and 14 clearly establish that these claims and claims dependent thereon are patentable over the prior art cited thus far and therefore no further prosecution on this application should be necessary. Applicants hereby request entry of the amendment pursuant to the provisions of Rule 116 as it obviates the need for any appeal or further action in this case.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-26 are in condition for allowance and notice to that effect is respectfully requested. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Inasmuch as this amendment is an Amendment after Final, the courtesy of a telephone call to Applicants' undersigned representative indicating entry of non-entry of the amendment is respectfully requested.

Respectfully submitted,

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